REMARKS

Applicant appreciates the Examiner's thorough examination of the subject application and requests reconsideration of the subject application based on the foregoing amendments and the following remarks.

Claims 1-13 are pending in the subject application. Claims 1-13 stand rejected under 35 U.S.C. §103.

35 U.S.C. §103 REJECTIONS

Claims 1-13 stand rejected under 35 U.S.C. §103 as being unpatentable over Suzuki et al. [USP 6,445,367; "Suzuki"] as provided on pages 2-4 of the above-referenced Office Action. Applicant respectfully traverses.

Applicant first provides a brief discussion of the present invention, so as to further the Examiner's understanding of the claimed invention and further the discussion as to why the presently claimed invention is distinguishable from the cited art. In a conventional signal reproduction circuit, all data was stored in a ROM, for example, for each type of control signal required to drive a display panel. For example, all data corresponding to HIGH and LOW was stored in a ROM for each of the four control signals Wl, W2, D1, D2. As a result, this required an extra large ROM capacity. Further, data was supplied from the ROM in the form of parallel data for each control signal, which required large numbers of output lines from the ROM. These factors posed problems with a conventional signal production circuit, including increased ROM size and cost to handle increased quantities of data, increased wire area for parallel

transfer of data, and increased substrate area. See page 4, line 19 to page 5, line 9 of the subject application.

Applicant claims, claim 1, a signal production circuit for producing a plurality of kinds of pulse signals as well as claims, claim 9, a display device including such a signal production circuit, which signal production circuit includes, *inter alia*:

(1) *storage means* for storing, as digital data, a single signal of serial data including a time series of data pulses representative of all rise and fall timings of the plurality of kinds of pulse signals and data pulses representative of all time intervals between the rise and fall timings; and

(2) *serial-to-parallel converter means* for reading the signal of serial data from the storage means and producing, as parallel data, the plurality of kinds of pulse signals from the data representative of all the predetermined rise and fall timings of the plurality of kinds of pulse signals.

The *serial-to-parallel converter means* converts single signals of serial data stored in the storage means to parallel signals to produce a plurality of kinds of pulse signals. The parallel conversion uses predetermined part of serial data representative of the rise and fall timings of each pulse signal and supplies produced pulse signals as parallel data via individual paths. The plurality of pulse signals include two or more kinds of pulse signals which may or may not have the same rise and fall timings. The serial data stored in the *storage means* is a time series of data representative of the rise and fall timings of the plurality of kinds of pulse signals. Therefore, the serial data can be arranged in any given manner, that is, pulse positions and widths as a signal can be

specified in any given manner; pulse signals with various rise and fall timings can be thus readily produced from the serial data.

Conventional serial-to-parallel converters do not change the total quantity of data before and after the conversion. As such, the quantity of data must be handled when serial data produced simply by linking data representative of pulse signals is read and converted to parallel data and when all data is stored in advance in storage means for each kind of pulse signal and read directly as parallel data. See also the *Background of the Invention* portion of the subject application.

The present invention differs from this. The present invention produces a single serial data by combining data representative of the rise and fall timings of each pulse signal and data representative of time intervals between all rise and fall timings arranged as a time series and stores the serial data in the *storage means*. Therefore, that part of the data which represents overlapping pulse signals as a time series can be omitted. This greatly reduces the total quantity of data stored in the *storage means*, compared to the storing of all data, and the required data transfer rate. Further, only single serial data must be read from the *storage means*. Therefore, the number of terminals and data output lines of the *storage means*, for example, ROM, can be reduced to one.

As a result, the data stored in a ROM or other *storage means* can be utilized more efficiently; the *storage means* becomes smaller in quantity and lower in cost. This reduces the size of the *storage means*, the wire area outside the *storage means*, and substrate area. See also page 6, line 13 to page 8, line 6 of the subject application.

The invention of Suzuki relates to such electron beam generating devices that prevent deviations and fluctuations in luminance and declines in contrast of an image display apparatus based on multiple electron beam sources equipped with cold cathode elements by rendering correct and fluctuation-free the intensity of electron beams emitted by the multiple electron beam sources (See column 5, lines 3-7 thereof). To this end, Suzuki determines the values of the current flows in n column wires on the basis of externally provided electron beam demand values, and actually supply the currents of those values to the column wires, while applying voltage V1 to selected ones of m row wires and voltage V2, different from voltage V1, to all the remaining row wires (See column 5, lines 12-29 thereof). As hereinafter discussed, Suzuki does not provide any description about storage means and serial-to-parallel converter means elements of the present invention.

The portion of Suzuki referred to in the above-referenced Office Action (e.g., column 13, lines 33-67, as well as Figs. 14 and 42 of Suzuki) describes the following five items.

1. The control circuit 103 coordinates the operation timing of each component so as to present an appropriate display, on the basis of an externally entered image signal.

2. The externally applied image signal may be a composite of image data and a synchronizing signal, as in the manner of an NTSC signal, or it may be a signal in which the image data and synchronizing signal are separated in advance.

3. The control circuit 103 generates control signals Tscan and Tmry for each component on the basis of an externally entered synchronizing signal Tsync.

4. Externally entered image data 5000 (luminance data) enters a shift register 104. Where the shift register 104 is for converting the image data, which enters serially in a time series, to a parallel signal every line of the image. The shift register 104 operates based on the control signal (shift clock) Tsft which enters from the control circuit 103.

5. The serial/parallel converted data of one line of the image (which data corresponds to the drive data of N-number of electron emission elements) is outputted to a latch circuit 105 as parallel signals I_{d1} to I_{dn}.

The Office Action asserts that the shift register 104 is used for converting the image data, which enters serially in a time series to a parallel signal every line of the image and thus, is equivalent to the *serial-to parallel converter means* of the present invention. The shift register 104 operates based on the control signal (shift clock) Tsft which enters from the control circuit 103. Therefore, comparing Suzuki with the present invention, the control circuit 103 thus should correspond to the storage means of the present invention.

The control circuit 103 in Suzuki, however, acts to coordinate the operation timing of each component so as to present an appropriate display on the basis of an externally entered image signal. Therefore, the control circuit 103 in Suzuki differs from the *storage means* of the present invention.

The Office Action admits that Suzuki does not specifically teach the use of data pulses including representations of all rise and fall timings along with the intervals

between those timings. Accordingly, the Office Action further states that Suzuki discloses a pulse-width modulating circuit 7111, a correction circuit 7489, and a LUT 7108 (see column 39, lines 59-67; and Fig. 42).

The pulse-width modulating circuit 7111, however, generates drive pulses having a pulse width corresponding to video signal intensity. The LUT 7108 stores leakage currents that flow out to elements other than a selected element at the time the panel is driven. The correction circuit 7489 corrects the amplitude of a drive voltage amount according to each column wire and the selected row and generates a constant-voltage pulse having this amount of voltage, by the use of the LUT 7108 and the voltage monitoring circuit 7111.

Therefore, the pulse-width modulating circuit 7111, the LUT 7108, and the correction circuit 7489 do not correspond to the *storage means for storing, as digital data, a single signal of serial data including a time series of data pulses representative of all rise and fall timings of the plurality of kinds of pulse signals and data pulses representative of all time intervals between the rise and fall timings.* Also, Suzuki is silent as to how the shift register 104 in Fig. 14 is related to the pulse-width modulating circuit 7111, the LUT 7108, and the correction circuit 7489 in Fig. 42. Therefore, it cannot be said that Suzuki is clear at all how these components/ circuits rely on each other for their operation. It is thus submitted that the *storage means* and the *serial-to-parallel converter means* of the present invention are not obvious from the shift register 104, the pulse-width modulating circuit 7111, the LUT 7108, and the correction circuit 7489 disclosed and taught in Suzuki.

The present invention also differs further from Suzuki in the following respects. The present invention efficiently uses data through the serial-to-parallel conversion process embodied in the signal production circuit and display device as claimed by Applicant. In contrast, in Suzuki, assuming that, for example, 10 data items are transferred from the control signal (shift clock) Tsft in the serial-to-parallel converter circuit between 103 and 104 in FIG. 14, 104 receives ten serial/parallel converted data items; not more, not less. In short, the total data quantity does not change before and after the conversion. It should be noted, however, that Suzuki is totally silent about the specific serial/parallel conversion method and its effects. Applicant thus believes that the circuitry and the like disclosed in Suzuki totally differs in nature from the signal productions circuit and display device as set forth in independent claims 1 and 9, respectively of the present invention.

In sum, the circuitry and the like described in Suzuki is totally different from the present invention in objectives and structure. Suzuki also does not provide any description, teaching or suggestion of the storage means and serial-to-parallel converter means as is claimed in the present invention. As such, the claims of the present invention are not obvious in view of Suzuki.

As provided in MPEP 2143.01, obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. *In re Fine*, 837 F. 2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); *In re Jones*, 958 F. 2d 347, 21

USPQ2d 1941 (Fed. Cir. 1992). As provided above, the cited reference includes no such teaching, suggestion or motivation.

Furthermore, and as provided in MPEP 2143.02, a prior art reference can be combined or modified to reject claims as obvious as long as there is a reasonable expectation of success. *In re Merck & Co., Inc.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 19866). Additionally, it also has been held that if the proposed modification or combination would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious. Further, and as provided in MPEP-2143, the teaching or suggestion to make the claimed combination and the reasonable suggestion of success must both be found in the prior art, not in applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). As can be seen from the forgoing discussion regarding the disclosures of the cited reference, there is no reasonable expectation of success provided in the reference or the admitted prior art.

As the USPTO Board of Patent Appeals and Interferences has held, "The mere fact that a worker in the art could rearrange the parts of the reference device to meet the terms of the claims on appeal is not by itself sufficient to support a finding of obviousness. The prior art must provide a motivation or reason for the worker in the art, without benefit of appellant 's specification, to make the necessary changes in the reference device." *Ex parte Chicago Rawhide Mfg. Co.*, 223 USPQ351, 353 (BD. Pat. App. & Inter. 1984).

It is respectfully submitted that for the foregoing reasons, claims 1-13 are patentable over the cited reference and satisfy the requirements of 35 U.S.C. §103. As such, these claims are allowable.

It is respectfully submitted that the subject application is in a condition for allowance. Early and favorable action is requested.

Applicant believes that additional fees are not required for consideration of the within Response. However, if for any reason a fee is required, a fee paid is inadequate or credit is owed for any excess fee paid, you are hereby authorized and requested to charge Deposit Account No. **04-1105**.

Respectfully submitted,
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